

Abstract

A thin stacked semiconductor device suitable for high speed operation. A plurality of specified circuits are formed on one surface of a semiconductor substrate while being arranged, and wiring and insulating layers being connected electrically with the circuits are laminated and formed sequentially in a specified pattern to form a multilayer wiring part. At the stage for forming the multilayer wiring part, a filling electrode is formed on the semiconductor substrate such that the surface is covered with an insulating film, a post electrode is formed on specified wiring at the multilayer wiring part, a first insulating layer is formed on one surface of the semiconductor substrate, the surface of the first insulating layer is removed by a specified thickness to expose the post electrode, the other surface of the semiconductor substrate is ground to expose the filling electrode and to form a through-type electrode, forward end of the through-type electrode is projected by etching one surface of the semiconductor substrate, a second insulating layer is formed on one surface of the semiconductor substrate while exposing the forward end of the through-type electrode, bump electrodes are formed on both electrodes and then the semiconductor substrate is divided to form a semiconductor device. A plurality of semiconductor devices thus obtained are stacked and secured at the bump electrodes thus manufacturing a stacked semiconductor device.